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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 03/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/030,175	DELEONIBUS, SIMON	
	Examiner	Art Unit	
	Ginette Peralta	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. (U. S. Pat. 6,271,094 B1) in view of Misra et al. (U. S. Pat. 5,960,270) and Ismail et al. (U. S. Pat. 5,955,759).

Regarding claim 1, Boyd et al. teaches in figs. 2A to 2F a method for fabricating an electronic component with self-aligned source, drain and gate, that comprises the steps of forming a dummy gate (52, 36) on a silicon substrate (10), the dummy gate defining a position for a channel (30) of the component, at least one implantation of doping impurities in the substrate, to form a source and a drain on either side of the channel, using the dummy gate as implanting mask (col. 7, ll. 12-15), superficial, self-aligned siliciding of the source and drain (col. 7, ll. 16-20), depositing at least one layer of insulating layer 60 and polishing the layer stopping at the dummy gate, replacing the dummy gate by at least one final gate separated from the substrate by a gate insulating layer62, and electrically insulated from the source and drain.

Boyd et al. shows all the limitations in the claim with the exception of forming a metal layer on the source, drain and dummy gate, selectively siliciding the metal layer on the source and drain; and depositing at least one layer of contact metal having a total thickness greater than the height of the dummy gate, and imparting an insulation characteristic to a surface region of the at least one contact metal layer and the metal layer on sides of the gate electrode.

Misra et al. discloses in Figs. 10-15 a method of fabricating an electronic component with a self-aligned source, drain and gate, wherein the process comprises the steps of forming a dummy gate 108 on a silicon substrate 102, said dummy gate defining a position for a channel of the component; at least one implantation of doping impurities, to form a source and drain 118 on either side of the channel, using the dummy gate as implanting mask; forming a metal layer on the source, drain and dummy gate (col. 9, lines 45-53); and superficial, self-aligned siliciding of the source and drain by selectively siliciding the metal layer on the source and drain (col. 9, lines 45-53), wherein the method comprises the forming of a metal layer on the source, drain, and dummy gate, followed by selective silicidation on the source and drain for the disclosed intended purpose of forming a metal gated metal oxide semiconductor transistor which contains self-aligned source and drain electrodes which are formed before forming the metal gate and have a reduced resistivity while avoiding adverse thermal processing of the metal gate.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a metal layer on the source, drain and dummy gate, and selectively siliciding the metal layer on the source and drain as Misra et al. teaches, in the invention of Boyd et al. for the disclosed intended purpose of forming a metal gated metal oxide semiconductor transistor which contains self-aligned source and drain electrodes which are formed before forming the metal gate and have a reduced resistivity while avoiding adverse thermal processing of the metal gate.

Ismail et al. discloses in figs. 9A to 9E a method of fabricating an electronic component with a self-aligned source, drain and gate that comprises the steps of forming a dummy gate on a silicon substrate, said dummy gate defining a position for a channel of the component; and after the source and drain regions have been formed, depositing at least one contact metal layer 15 having a total thickness greater than a height of the dummy gate 1, polishing the contact metal layer stopping at the dummy gate, and imparting an insulation characteristic to a surface region 17 of the at least one contact metal layer and the metal layer on sides of the gate electrode as taught in col. 5, lines 12-48, wherein the contact metal layer is deposited, polished and modified to impart an insulation characteristic to a surface region for the disclosed intended purpose of forming a contact to the source and drain regions and protecting the source and drain contacts from further processing.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to deposit a contact metal layer, polish the contact metal layer

stopping at the dummy gate and imparting an insulation characteristic to a surface region of the contact metal layer in the invention of Boyd et al. for the disclosed intended purpose of Ismail et al. of forming a contact to the source and drain regions and protecting the source and drain contacts from further processing.

Regarding claim 2, Boyd et al, as modified by Ismail et al. above teaches depositing a first metal layer 6, and above the first layer, a second metal layer 17 having greater mechanical resistance to polishing than the first layer, the thickness of the first metal layer 6 being less than the height of the dummy gate, but the total thickness of the first and second layers being greater than the height of the dummy gate.

Regarding claim 3, Boyd et al. teaches in col. 8, ll. 6-10, forming the side spacers 32 on the sides of the dummy gate before siliciding.

Regarding claim 5, Boyd et al. as modified by Ismail et al. above, teaches the first metal comprising titanium or tungsten, and the second metal comprising tungsten or titanium nitride.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any other refractory material like tantalum, titanium, or molybdenum, among others, and alloys thereof, as the use of this materials is well known in the art and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Regarding claim 6, Boyd et al. as modified by Ismail et al. teaches that the surface insulation comprises superficially oxidizing the contact metal layer (col. 5, lines 41-48).

Regarding claim 7, Boyd et al. teaches the use of a solid substrate.

Regarding claim 8, Boyd et al. does not specify the substrate used. Misra et al. teaches the use of silicon on insulator substrate as well as silicon substrates and other semiconductor substrates, and further teaches that any of these substrates may be used for fabricating an electronic component having a self-aligned source, drain and dummy gate. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use any type of semiconductor substrate like SOI or silicon, among others, as the use of this substrates is well known in the art as shown by Misra et al..

Regarding claim 9, Boyd et al. teaches that the step of removal of the dummy gate includes formation of a gate insulation layer 62, depositing a metal layer 28 as the gate layer, having an overall thickness equal to or greater than the height of the removed dummy gate, and forming the metal layer.

Regarding claim 11, Boyd et al. as modified by Ismail et al. above discloses that the surface insulation comprises depositing a layer of dielectric material.

Regarding claim 4, Boyd et al. as modified by Misra et al. teaches a method of manufacturing a MOSFET utilizing a dummy gate, that discloses in fig. 12 dual-layer spacers that are formed comprising an attachment layer 112 of silicon oxide in contact with the dummy gate, and a superficial layer 114 comprising silicon nitride, wherein a

dual layer is used as the spacers for the purpose of protecting the gate structure in further process steps.

Thus, it would have been within the scope of one of ordinary skill in the art at the time the invention was made to use a dual-layer as the one taught by Misra et al. for its intended purpose of protecting the gate electrode structure. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a single or dual-layer spacers, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson*, 136 USPQ 184.

3. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boyd et al. in view of Misra et al. and Ismail et al. as applied to claims 1-9, and 11 above, and further in view of Gardner et al. (U. S. Pat. 6,200,865 B1).

Boyd et al. as modified by Deleonibus above teaches all the limitations in the claim with the exception of depositing an inter-gate dielectric layer and a second gate metal layer.

Gardner et al. teaches a method of manufacturing a semiconductor device that includes the formation of a gate insulating layer 36, the deposition of a first gate metal layer 46, the deposition of one inter-gate dielectric layer 50, and the deposition of a second gate metal layer 56, wherein the structure is formed in this manner for the disclosed intended purpose of forming a dual gate structure that is useful in memory cells by decreasing the area of the device.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dual gate comprising a first and second metal layers, and an inter-gate dielectric in the invention of Boyd et al. for the disclosed intended purpose of Gardner et al. of forming a structure that decreases the size of the device by providing a dual gate that can be useful in memory devices.

Response to Arguments

4. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (571)272-1713. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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